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Silicon VLSI Technology: Fundamentals, Practice, And Modeling

SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling

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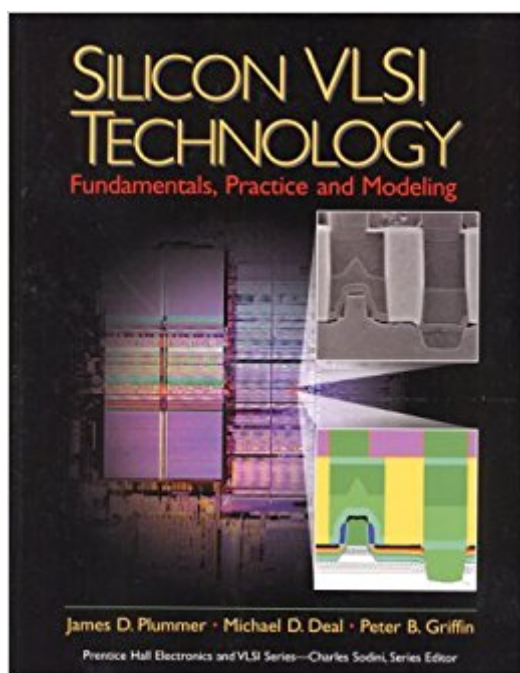
Synopsis

Unique in approach, this book provides an integrated view of silicon technology--with an emphasis on modern computer simulation. It describes not only the manufacturing practice associated with the technologies used in silicon chip fabrication, but also the underlying scientific basis for those technologies.   Modern CMOS Technology. Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers. Semiconductor Manufacturing--Clean Rooms, Wafer Cleaning and Gettering. Lithography. Thermal Oxidation and the Si/SiO2 Interface. Dopant Diffusion. Ion Implantation. Thin Film Diffusion. Etching. Backend Technology.   For anyone interested in Fabrication Processes.

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Customer Reviews

Unique in approach, this book provides an integrated view of silicon technology—with an emphasis on modern computer simulation. It describes not only the manufacturing practice associated with the technologies used in silicon chip fabrication, but also the underlying scientific basis for those technologies. FEATURES/BENEFITS   Extensive use of modern computer simulation methods and examples—Integrated into each chapter. Illustrates how technologies work. Allowing the reader to develop a better physical understanding of concepts and helps them in visualizing features of the technologies that are not easily seen any other way.   Early, broad exposure to a complete chip manufacturing process (Ch. 2).   Ties many diverse processing concepts together and establishes the context for the specific technologies discussed in later chapters.   Examples of modern manufacturing practice.   Providing readers with practical examples

of fundamental concepts.   Historical perspective and introduction.   An integrated view of silicon technology—with an emphasis on modern computer simulation.   Extensive use of modern computer simulation methods and examples—integrated into each chapter. Early, broad exposure to a complete chip manufacturing process. Examples of modern manufacturing practice.

Preface   The silicon integrated circuit is surely one of the wonders of our age. The ability to fabricate tens of millions of individual components on a silicon chip with an area of a few cm2 has enabled the information age.   Basic discoveries and inventions between 1945 and 1970 laid the foundations for these chips. In the past 30 years, chip complexity has increased at an exponential rate, primarily because of the constant shrinking of device geometries, improved manufacturing practice, and clever inventions enabling specific functions to be implemented in new ways. Shrinking geometries permit more devices to be placed in a given area of silicon; improved manufacturing permits larger chips to be economically fabricated; and clever inventions permit functions to be realized in smaller areas. It is widely expected that these historical trends will continue for at least another 10-20 years, resulting in chips that contain billions of components. Such chips will have extraordinary capabilities. We will likely find ourselves in 10-20 years thinking of today's chips as primitive precursors to the chips that will be in manufacturing at that time.   The technology that is used to build silicon integrated circuits today has evolved largely through empirical methods. It often seems that the chip industry moves so rapidly and new products are introduced so often that there is little time to worry about the scientific basis of the technologies used to build these chips. Yet in parallel with the rapid pace of this industry, a strong effort has been proceeding, often behind the scenes, to develop a solid, physically based understanding of the many technologies used in chip manufacturing. Because of the feature sizes of structures in modern chips, this understanding often needs to be on a molecular or atomic level. It is not sufficient any longer to think of silicon oxidation as simply a chemical reaction between silicon and oxygen that grows SiO2. Today we must understand the detailed bonding between silicon and oxygen atoms and the kinetics that drive this reaction on an atomic basis.   Silicon integrated circuit technology makes use of many diverse fields of science and engineering. The optical steppers which print microscopic patterns on wafers, represent one of the most advanced applications of the principles of Fourier optics. Plasma etching involves some of the most complex chemistries used in manufacturing today. Ion implantation draws upon understanding from research in high energy physics. Thin films on the silicon wafer surface exhibit complex mechanical behavior which stretches our understanding of basic materials properties. And of course, silicon devices themselves are approaching physical sizes at which molecular and atomic

scale phenomena involving ideas from quantum mechanics are important. One of the great challenges in integrated circuit manufacturing is the need to draw on scientific principles and engineering developments from such an extraordinarily wide range of disciplines. Integrating the knowledge from these diverse disciplines has been and will continue to be a great challenge. Scientists and engineers who work in this field need broad understanding and this ability to seek out, integrate and use ideas from many fields.   Over the past 20 years much has been learned about silicon and the other materials that are used in modern chips. Often new knowledge is incorporated in a "model" which may be a mathematical equation describing a process or an atomistic picture of how particular process works. Models codify knowledge and are an elegant way of expressing what is known. They also provide a way of exchanging ideas between researchers in a particular field, and can be tested experimentally to assess their predictive capability.   Within the last decade, a serious attempt has been made to develop computer simulation tools which can simulate the various technologies used in fabricating chips. These simulation tools are built around models of the physical processes involved. Some simulation tools today use well-established scientific principles to predict experimental results. Optical lithography simulators, which are based on mathematical descriptions of Fourier optics, are a good example. Such tools today can accurately predict the image that will be printed in resist on a silicon wafer, given a particular mask design and a specific exposure system. Other simulation tools rest on less solid ground. Models of dopant diffusion in silicon, for example, use models which are still debated in the scientific community and which are clearly incomplete in terms of describing all the physical phenomena involved. Nevertheless, even these models are very useful today.   This book attempts to describe not only the manufacturing practice associated with the technologies used in silicon chip fabrication, but also the underlying scientific basis for those technologies. Those scientific principles are described in terms of models of the process in many cases. In most chapters, models are discussed in the context of computer simulation programs which have incorporated the models and which use them to simulate technology steps. We make extensive use of simulation examples to illustrate how technologies work and to help in visualizing features of the technologies that are not easily seen any other way. We have found these tools to be powerful teaching aids.   Simulation tools are widely used in the semiconductor industry today to supplement traditional experimental methods. While it is unlikely that simulation will completely eliminate the need for experiments, especially in a fast moving industry like the IC industry, simulators can result in very substantial cost savings in developing new generations of technology and in solving manufacturing problems. It is widely believed that simulation tools will be essential in the future if the rapid progress that has

characterized the semiconductor industry is to continue.   This book is organized somewhat differently than other texts on this general topic, in two principal ways. The first is the extensive use of simulation examples throughout the text. These serve several purposes. The first is simply to help explain the scientific principles involved in each chapter. Simulations help to illustrate things like the time evolution of a growing oxide layer, a diffusing dopant profile or a depositing thin film. They are also very useful in illustrating the effects of specific physical phenomena in a process step because it is straightforward in simulators to add or eliminate specific physical models. Simulators provide the only real way in which complex interactions between process steps can be illustrated and understood. Finally, students who spend their careers in this industry will certainly use these tools and understanding their capabilities and limitations will be important in their future work.   The second way in which this book is organized differently is the discussion of a complete process flow early in the book (Chapter 2). While readers new to this field may not appreciate many of the complexities of a CMOS process before studying the later chapters, we have found that an early broad exposure to a complete chip manufacturing process is very helpful in establishing the context for the specific technologies discussed in later chapters. In teaching the material in this book, we usually cover the CMOS process in the first or second lecture somewhat superficially, and then return to the same topic in the last lecture, at which point the details can be more fully discussed. We have also attempted in each chapter to include some discussion of future trends. Predicting the future is obviously difficult and there is some risk that including this material will simply serve to date this book. Nevertheless, we have found that students are often interested in this topic and at least in general terms, we believe it is possible to predict where silicon technology is heading. The semiconductor industry National Technology Roadmap for Semiconductors (the NTRS) provides some guidance in looking to the future.   The material in this book can be covered in a one quarter senior/graduate level course, although not all of the material in each chapter can be covered in one quarter. A semester long course would provide more time to cover the full range of material in the book. If the book is used in connection with a one quarter long course, one option is to minimize the amount of time spent on the Manufacturing Methods and Measurement Techniques sections in each chapter. A set of lecture notes based on figures from the text is available to instructors by contacting the publisher or the authors by email. We have used these notes several times in a one quarter course at Stanford.   Follow-on courses to a basic IC fabrication course can make more extensive use of the simulation tools discussed in this text. We have not used the simulation tools described in this book for homework assignments or for lab assignments in connection with a first course in IC fabrication. We believe that the simulation examples are better used simply as teaching

tools in such courses, to illustrate ideas and to clarify physical principles. But in a follow-on course, hands-on experience with these simulation tools is easily possible. Most of the computer tools we use in the book are commercially available and the vendors of these tools are generally anxious to work with university instructors to make the tools available for teaching purposes. Finally, we acknowledge the many students at Stanford who have helped refine the material in this book by using various draft versions of the text in classes we have taught. Their inputs and suggestions have hopefully made this a better book. For many years we have worked with an energetic group of Ph.D. students and faculty colleagues at Stanford who have helped to develop some of the models and software tools described in this book. We particularly acknowledge Professor Bob Dutton and former Ph.D. students Professor Mark Law (now at the U. Florida) and Dr. Conor Rafferty (now at Lucent Technologies). We are also very grateful to a number of individuals who reviewed draft versions of this book and who provided technical inputs to various chapters. Paul Rissman of Hewlett Packard, Jim McVittie of Stanford, and Mark Law all provided substantial inputs and comments. Our own work in this field has been reported over many years by DARPA (the Defense Advanced Research Projects Agency) and by the Semiconductor Research Corporation (SRC) . We owe them a considerable debt of gratitude for making our work possible. We welcome comments; suggestions on this text by email at plummer@ee.stanford.edu, deal@ee.stanford.edu, griffin@stanford.edu.

The book itself is great. Good content.But, the paper quality of the book is terrible. Some letters are not even readable. Paperback for this price is rip off. I've taken James Plummer's class. Even he couldn't believe the ripoff price of the paperback book. Don't buy it. Also, the cover of the book has directly started to wear off. The pages can separate anytime if I use the book a little bit more.

A superbly written book on fabrication of silicon integrated circuits.Chapter 2 provides a gentle yet fairly detailed introduction to the overall process and each item touched therein is expanded subsequently.The language is clear and figures convey their intended meaning,overall its a wonderful starting point for further study in silicon integrated circuits technology.As has been pointed out in one of the reviews here, this book has been adopted in many US universities.The link embedded in this review is one such instance and as such can be used to obtain more information and benefit from a full set of audio lectures, assignemnts and other supplementary material as a part of MIT's open course ware program.The instructor is Prof Judy Hoyt.[...]

The text is a classic, and the material is thoroughly and competently covered, even if slowly becoming dated. However, the quality of production of this text is awful! Be warned: this is a facsimile. The resolution of the pictures and text is horrible. In many cases, parts of equations and diagrams are unreadable. Literally, it looks like a poorly scanned copy that someone printed on a cheap home laser printer, and the quality is the same as if one had done this. Many of the figures are useless because of thisWhat is more, there is very little margin on the right half of even pages. This means that you cannot normally read most of the right side of the paragraph, as the text goes almost into the spine of the book. You have to constantly tilt the book, move your head closer, and struggle to read this text. You may say to yourself, "No problem. I will just crack open the book wider." Well, that is exactly what will happen: your book will crack! The glue in the binding is so cheap that pages started falling out of my book after light use. Trying to open it even the slightest will eventually rip the book apart. And you need to open it very widely because of the thickness of the cheap paper. The hardcover is only about one third of the thickness of this version.I expected more for the $145 that was charged for this text. My advice: get another copy (perhaps an old hardcover) that is of higher quality.

Good book for the undergrads. Covers most of the VLSI aspects, a nice book to have in your library. The problems given at the end of each chapter are to help increase your understanding of the content. Don't Don't Don't ignore them.

if your an electrical / process engineer, this is one of the must have books.

Binding of the book is very bad that you cannot open the book completely or even cannot see end of the lines. And paper quality is poor.

I've read a number of books in this field - Plummer, Wolf, Campbell, Sze, Madou. Each book has its strength, and Plummer's book stands out in terms of its broad, in-depth coverage of modern silicon CMOS technology. It doesn't cover MEMS or other exotic nanofabrication.Many students who've read the book said that Chap 2, where a modern CMOS process flow is described step by step from the substrate to back-end, was the best part. By doing so, the authors teach us that not only unit processes but their collection, i.e. process integration, is the key in successful CMOS technology. Overall, the quality of the content and attention to small details are superb, as one can expect from a book written by one of world's foremost researchers in the field (Plummer is the Dean of

Engineering School at Stanford). In particular, I liked chap2 for integrated description of CMOS flow, the lithography chapter which covers optical systems, details of photoresists, phase shift masking. Also, diffusion and ion implantation parts are second to none, since the authors made numerous contributions to the research field. It's such pleasure to learn about the latest in silicon IC processing from the Silicon Valley authority at Stanford! The book has been adopted by many US engineering schools already, and I see it on many bookshelves belonging to IC engineers. If you need an authoritive, well-organized reference for modern silicon IC processing, I strongly recommend this book.

If you are a process engineer, or want to become one, this book is a must have. Like other reviewers said, chapter 2 lays a context for the chapter ahead. From being a zero in basics, I went to become a person who could answer questions regarding fundamentals with ease and comfort, and build on those basics easily. All of that credit certainly goes to the way Mr. Plummer laid-out his textbook. Simple explanations of complex fundamentals, supported with pictures, flow-diagrams and drawings make this book not only interesting to read, but also an essential reference.I would definitely recommend this book if you want to learn or strengthen your IC fabrication fundamentals! Happy reading!

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